CLAIMS

1. (Currently amended) A flat-type capacitor comprising:

a lower interconnection on a predetermined portion of a semiconductor substrate;

a lower electrode that has ~~a flat shape~~ an overall shape that is substantially flat, the lower electrode electrically coupled to the lower interconnection, the lower interconnection disposed below the lower electrode;

a concave dielectric layer disposed on the lower electrode;

a concave upper electrode disposed on the dielectric layer, a length of a bottom part of the concave upper electrode greater than a length of the lower electrode;

a first upper interconnection that is electrically coupled to the lower interconnection; and

a second upper interconnection that is coupled to the first upper interconnection.

2. (Original) The capacitor of claim 1, wherein the lower electrode is positioned between edges of the concave upper electrode.

3. (Original) The capacitor of claim 1, wherein the lower electrode and the upper electrode are composed of a material selected from the group consisting of Ti, Ta, W, TiN, TaN, Al, Cu, Ru, Pt, Ir, and combinations thereof.

4. (Previously presented) The capacitor of claim 1, wherein the dielectric layer is composed of a material selected from the group consisting of SiO_2, Si_3N_4, Ta_2O_5, Al_2O_3, HfO, ZrO_2, $BaSrTiO_3$, $PbZrTiO_3$, and $SrTiO_3$.

5. (Previously presented) A flat-type capacitor comprising:

a first metal interconnection disposed on a predetermined surface of a semiconductor substrate;

a first interlayer dielectric disposed on the first metal interconnection and the semiconductor substrate;

a second interlayer dielectric disposed on the first interlayer dielectric;

a lower electrode disposed on the first interlayer dielectric and coupled to one side of the first metal interconnection;

a second metal interconnection disposed on the first interlayer dielectric and electrically isolated from the lower electrode;

a third interlayer dielectric disposed on the second interlayer dielectric;

a concave dielectric layer disposed on the lower electrode and the second interlayer dielectric;

a concave upper electrode disposed along a top surface of the concave dielectric layer, a length of the concave upper electrode greater than a length of the lower electrode;

a fourth interlayer dielectric disposed on the concave dielectric layer, the concave upper electrode, and the third interlayer dielectric; and

third metal interconnections disposed on the fourth interlayer dielectric, wherein one of the third metal interconnections is coupled to the upper electrode and another one of the third metal interconnections is coupled to the second metal interconnection.

6. (Original) The capacitor of claim 5, wherein the lower electrode is positioned between edges of the concave upper electrode.

7. (Original) The capacitor of claim 5, wherein the upper electrode and the second metal interconnection are formed of the same material.

8. (Original) The capacitor of claim 7, wherein the lower electrode, the second metal interconnection, and the upper electrode comprise material selected from the group consisting of Ti, Ta, W, TiN, TaN, Al, Cu, Ru, Pt, Ir, and combinations thereof.

9. (Original) The capacitor of claim 5, wherein the lower electrode, the second metal interconnection, and the second interlayer dielectric have the same thickness.

10. (Previously presented) The capacitor of claim 5, wherein the dielectric layer comprises a material selected from the group consisting of SiO_2, Si_3N_4, Ta_2O_5, Al_2O_3, HfO, ZrO_2 $BaSrTiO_3$, $PbZrTiO_3$, and $SrTiO_3$.

11. (Original) The capacitor of claim 10, wherein the first, second, third, and fourth interlayer dielectrics have the same etch selectivity.

12-30. (Cancelled)

31. (Currently amended) A capacitor comprising:

a lower interconnection on a predetermined portion of a semiconductor substrate;

a lower electrode that is electrically coupled to the lower interconnection and that is disposed above the lower ~~interconnection, the lower electrode having substantially horizontal surfaces and substantially vertical surfaces, a total area of the substantially horizontal surfaces greater than a total area of the substantially vertical surfaces~~ interconnection, the lower electrode having an overall shape that is substantially flat in cross-section;

a concave upper electrode having ~~a lowermost horizontal surface, a total area of the lowermost horizontal surface greater than a total area of an uppermost horizontal surface of the lower electrode;~~ an overall shape that is substantially U-shaped in cross-section;

a concave dielectric layer disposed in contact with the lower electrode and the concave upper electrode;

a first upper interconnection that is electrically coupled to the lower interconnection; and

a second upper interconnection that is coupled to the first upper interconnection.

32. (New) The capacitor of claim 31, the concave upper electrode having a lowest horizontal surface that is disposed at a level that is vertically higher than a highest horizontal surface of the lower electrode.

33. (New) The capacitor of claim 32, the lowest horizontal surface longer than the highest horizontal surface by a predetermined amount, the lowest horizontal surface wider than the highest horizontal surface by the predetermined amount.